INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number		09452328	
Filing Date		1999-11-30	
First Named Inventor	Swain W. Porter		
Art Unit		2152	
Examiner Name	Chankong, Dohm		
Attorney Docket Number		112076-138323	

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

That no item of information contained in the information disclosure statement was cited in a communication from a
foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification
after making reasonable inquiry, no item of information contained in the information disclosure statement was known to
any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure
statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

X None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Steven J. Prewitt/	Date (YYYY-MM-DD)	2008-05-19
Name/Print	Steven J. Prewitt	Registration Number	45023

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

PAT-NO:

JP401044049A

DOCUMENT-IDENTIFIER: JP 01044049 A

TITLE:

ELECTRODE FOR FLIP CHIP BONDING

PUBN-DATE:

February 16, 1989

INVENTOR-INFORMATION:

NAME

NOBUHARA, HIROYUKI

ASSIGNEE-INFORMATION:

NAME

COUNTRY

FUJITSU LTD

N/A

APPL-NO:

JP62201332

APPL-DATE:

August 12, 1987

INT-CL (IPC): H01L021/92

US-CL-CURRENT: 438/614, 438/FOR.343

ABSTRACT:

PURPOSE: To prevent a fusion-bonding metal and a wiring layer from reacting by providing a barrier layer made of diffusion preventing metal or insulator of a fusion-bonding metal layer also on the side face of the metal.

CONSTITUTION: An AuSn fusion-bonding metal layer 6 is formed as a bump through an Ni layer or a Pt/Ti layer as a barrier layer 5 made of the diffusion preventing metal of the fusion-bonding metal at an electrode forming position on an Au/AuGe ohmic contact electrode 3 formed on an N-type InP substrate 1. Then, an Ni layer 8 is deposited on a whole substrate, covered with an AZ resist, patterned to allow an AZ resist pattern 10 to remain on the periphery of the electrode. Thereafter, the pattern 10 is etched back by reactive ion